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APPLICATION FOR UNITED STATES LETTERS PATENT

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STRAINED DISLOCATION-FREE CHANNELS FOR CMOS AND METHOD OF MANUFACTURE

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device and method of manufacture which imposes tensile and compressive stresses in the device during device fabrication.

Background Description

Mechanical stresses within a semiconductor device substrate can modulate device performance. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the n-type devices (e.g., NFETs) and/or p-type devices (e.g., PFETs). However, the same stress component, either tensile stress or compressive stress, discriminatively affects the characteristics of an n-type device and a p-type device.

In order to maximize the performance of both nFETs and pFETs within integrated circuit (IC) chips, the stress components should be engineered and applied differently for

nFETs and pFETs. That is, because the type of stress which is beneficial for the performance of an nFET is generally disadvantageous for the performance of the pFET. More particularly, when a device is in tension (e.g., in the direction of current flow in a planar device), the performance characteristics of the nFET are enhanced while the performance characteristics of the pFET are diminished. To selectively create tensile stress in an nFET and compressive stress in a pFET, distinctive processes and different combinations of materials are used.

For example, a trench isolation structure has been proposed for forming the appropriate stresses in the nFETs and pFETs, respectively. When this method is used, the isolation region for the nFET device contains a first isolation material which applies a first type of mechanical stress on the nFET device in a longitudinal direction (e.g., parallel to the direction of current flow) and in a transverse direction (e.g., perpendicular to the direction of current flow). Further, a first isolation region and a second isolation region are provided for the pFET and each of the isolation regions of the pFET device applies a unique mechanical stress on the pFET device in the transverse and longitudinal directions.

Alternatively, liners on gate sidewalls have been proposed to selectively induce the appropriate stresses in the channels of the FET devices (see, Ootsuka et al., IEDM 2000, p.575, for example). By providing liners the appropriate stress is applied closer to the device than the stress applied as a result of the trench isolation fill technique.

While these methods do provide structures that have tensile stresses being applied to the nFET device and compressive stresses being applied along the longitudinal direction of the pFET device, they may require additional materials and/or more complex processing, and thus, resulting in higher cost. Further, the level of stress that can be applied in these situations is typically moderate (i.e., on the order of 100s of MPa). Thus, it is desired to provide more cost-effective and simplified methods for creating large tensile and compressive stresses in the channels nFETs and pFETs, respectively.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a method is provided for manufacturing a semiconductor structure. The method includes forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate. A first layer of material is provided within the pFET channel having a lattice constant different than the lattice constant of the substrate and a second layer of material is provided within the nFET channel having a lattice constant different than the lattice constant of the substrate. An epitaxial semiconductor layer is formed over the first layer of material in the pFET channel and the second layer of material in the nFET channel. The epitaxial semiconductor layer has substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel.

In another aspect of the invention, a method of manufacturing a semiconductor structure is provided. The method includes forming a pFET and an nFET channel in a

substrate layer such as Si or silicon on insulator. A first layer of material is provided within the pFET channel having a lattice constant different than the lattice constant of the substrate layer and a second layer of material is provided within the nFET channel having a lattice constant different than the lattice constant of the substrate layer. An epitaxial semiconductor layer is formed over the first layer of material in the pFET channel and the second layer of material in the nFET channel. The epitaxial semiconductor layer has substantially a same lattice constant as the substrate layer thus creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel.

In still a further aspect of the invention, a semiconductor structure includes a pFET and nFET channel formed in a substrate such as, for example, a Si layer. A shallow trench isolation structure is formed in the Si layer and a first layer of material in the pFET channel having a lattice constant different than the lattice constant of the Si layer. A second layer of material in the nFET channel has a lattice constant different than the lattice constant of the Si layer. An epitaxial semiconductor layer formed over the first layer of material in the pFET channel and the second layer of material in the nFET channel has substantially a same lattice constant as the Si layer thus creating a desired stress component within the pFET channel and the nFET channel.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a through 1f represent a fabrication process to form a device in accordance with the invention;

Figures 2a through 2d represent a fabrication process to form a device in accordance with the invention;

Figure 3 illustrates the locations of the stresses in an nFET device according to the invention; and

Figure 4 illustrates the locations of the stresses in a pFET device according to the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

This invention is directed to a semiconductor device and method of manufacture which provides tensile stresses in the nFET channel and compressive stresses in the pFET channel of CMOS devices. In one embodiment, high tensile stresses may also be provided in the pFET channel to increase device performance. In one embodiment of the invention, channels are formed in the silicon layer in the area of the formation of the nFETs and pFETs. The channels are then filled with silicon based material having a naturally occurring lattice constant which does not match the lattice constant of the underlying silicon layer. By applying these materials, tensile and/or compressive forces result in an overlying epitaxial layer in the channels of the nFETs and pFETs, respectively. In one embodiment, the nFET and pFET channels can be formed

simultaneously. By using the fabrication processes of the invention, improved device characteristics can be achieved, as well as higher yields and lower device defects. Also, lower manufacturing costs can be realized with the fabrication processes of the invention.

Figures 1a through 1f represent a fabrication process to form a device in accordance with the invention. In Figure 1a, a substrate 10 such as, for example, silicon-on-insulator (SOI) or the like is provided. It includes a buried oxide layer 15 and a Si-on-insulator layer 20 (e.g., Si layer). The SOI wafer could be formed by either SIMOX or bonded techniques that are well known in the art. In one embodiment, the Si layer 20 is approximately 300 Å to 1500 Å; however, it should be well understood that variations in the height of the Si layer 20 are contemplated by the invention depending on the particular application.

Still referring to Figure 1a, the Si layer 20 is then patterned to form shallow trench isolation features (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE) of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art. The pad nitride is then stripped.

Now referring to Figure 1b, an oxide layer 32 is deposited on the polished surface of the STI regions 25 and the Si layer 20. The height of this oxide layer 32 may vary and is, in one embodiment, approximately 200 Å. A photo resist layer 35, which can be any known photo resist material, is deposited on the oxide layer 32. After using known

masking and lithographic patterning techniques, a reactive ion etching, for example, is then performed on the photo resist layer 35 and the oxide layer 32. The reactive ion etching, in this step, may be selective to the oxide layer. This begins the process of forming the pFET channels 40 and the nFET channels 45, simultaneously. After the oxide etch, the Si layer 20 is selectively etched using a reactive ion etch, as shown in Figure 1c.

In an alternative step, the Si is first amorphized using a Ge implant at a typical dose of 2e14#/cm^2 to 1e15 #/cm^2 with an energy in the range of 10keV to 100keV depending on the depth of etches needed. This optional amorphization step may be used to improve the etch quality. In either fabrication, the channels 40 and 45 are formed in the Si layer 20 corresponding to a placement of the pFETs and nFETs, respectively. In one implementation, the channels 40 and 45 are etched to a depth of about 200Å to 400Å, in the Si layer 20. However, this depth may vary depending on the particular application used with the invention.

Figure 1d is representative of further fabrication processes in accordance with the invention. In these fabrication processes, the photo resist material 35 is removed using any known processes. A hard mask 50 is patterned within the pFET channel 40 using any known lithographic process. In one embodiment, the hard mask is a Nitride material and is patterned over the oxide layer 32, proximate the pFET channel 40. A SiGe layer 45a is epitaxial grown in the nFET channel 45 to a thickness of about 100 Å to 300 Å, although other thicknesses are also contemplated by the invention.

Standing alone, the SiGe normally has a larger lattice constant than the Si layer 20. That is, the lattice constant of the SiGe material does not match the lattice constant of the Si layer 20. However, in the structure of the invention, due to the growth of the SiGe layer 45a within the nFET channel 45, the lattice structure of the SiGe layer 45a will tend to match the lattice structure of the underlying Si layer 20.

By virtue of the lattice matching of the SiGe 45a (which normally is larger) to the Si layer 20, this results in the SiGe layer 45a and the surrounding areas being under compression. The surrounding areas of the SiGe layer, though, will try to obtain an equilibrium state thus resulting in a tensile stress of an epitaxial Si layer formed on the SiGe layer 45a (as shown in Figure 1f). In one embodiment, the Ge content of the SiGe layer 45a may be from 5% to 50% in ratio to the Si content.

In Figure 1e, the hard mask 50 is removed by any known process. A hard mark 55 is patterned within the nFET channel 45 using any known lithographic process. The hard mask 55 is also patterned over the oxide layer 32, proximate to the nFET channel 45 and over the thus grown SiGe layer 45a. Again, in one embodiment, the hard mask 55 is a Nitride material. A Si:C layer 40a is then epitaxial grown in the channel 40 of the pFET to a thickness of about 100 Å to 300 Å, although other thicknesses are also contemplated by the invention. It should be understood by those of ordinary skill in the art that the process steps of Figure 1e may equally be performed prior to the process steps shown in Figure 1d.

Standing alone, Si:C would normally have a smaller lattice constant than the Si layer 20. That is, the lattice constant of the Si:C material does not match the lattice constant of the Si layer 20. However, in the structure of the invention, due to the growth of the Si:C layer 40a within the pFET channel 40, the lattice structure of the Si:C layer 40a will tend to match the lattice structure of the underlying Si layer 20.

By virtue of the lattice matching of the Si:C 40a (which normally is smaller) to the Si layer 20, this results in the Si:C layer 40a and the surrounding areas being under a tensile stress. Similar to the occurrence with the SiGe layer, the surrounding areas of the Si:C layer 40a will try to obtain an equilibrium state thus resulting in a compressive stress of an epitaxial Si layer formed on the Si:C layer 40a. In one embodiment, the C content may be from 0% to 4% in ratio to the Si content.

Figure 1f shows an intermediate structure. To obtain this structure, the hard mask 55 is removed, in a similar fashion to that described with reference to Figure 1e. A Si epitaxial layer 60 is selectively grown over the Si:C and SiGe layers in channels of the pFETs and nFETs, respectively. In an embodiment, the Si epitaxial layer 60 equilibrates with the surrounding structure of SiGe 45a or Si:C 40a and the Si insulation layer 20 resulting in a tensile stress in the nFET channel 45 and a compressive stress in the pFET channel 40, as discussed above. It should be understood that by adjusting the concentrations of the Ge content in the SiGe layer, it is possible to adjust the tensile stress in the nFET channel 45. Similarly, by adjusting the concentrations of C in the Si:C layer, it is possible to then adjust the compressive stress in the pFET channel 40. This is due to the lattice constant of such materials.

Still referring to Figure 1f, a sacrificial oxide layer 65 is then grown over the selectively grown epitaxial Si layer 60. Then the pFET is masked using standard photoresist-based lithographic techniques so that the nFET channel implants can be performed. After stripping the related photoresist (not shown in the Figure 1f) the nFET is then masked (again using standard photoresist-based lithographic techniques) and the pFET channel implants are performed followed by another photoresist strip. Then, the sacrificial oxide layer 65 is stripped and the gate oxidation layer 70 is grown as shown in Figure 1f. Then, the gate polysilicon 70 is formed in the pFET and nFET regions. The gate poly deposition and chemical mechanical polishing, well known to those of ordinary skill in the art, is performed to produce the structure shown in Figure 1f.

After stripping the damascene oxide layer 32, standard CMOS processing may continue the process. For example, after the oxide layer 32 is stripped using any known process, standard spacer and ion implantation processes can be performed to form the extensions and source and drain regions of the pFETs and nFETs.

Figures 2a through 2d represent another fabrication process to form a device in accordance with the invention. In Figure 2a, the substrate and STI are formed in the same way as that for Figure 1a. . In Figure 2a, a substrate 10 such as, for example, silicon-on-insulator (SOI) or the like is provided. It includes a buried oxide layer 15 and a Si-on-insulator layer 20. The SOI wafer could be formed by either SIMOX or bonded techniques that are well known in the art. In one embodiment, the Si layer 20 is approximately 300 Å to 1500 Å; however, it should be well understood that variations in

the height of the Si layer 20 are contemplated by the invention depending on the particular application.

Still referring to Figure 2a, the Si layer 20 is then patterned to form shallow trench isolation features (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE) of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art. The pad nitride is then stripped.

Now referring to Figure 2b, an oxide layer 32 is deposited on the polished surface of the STI regions 25 and the Si layer 20. The height of this oxide layer 32 may vary and is, in one embodiment, approximately 200 Å. A photo resist layer 35, which can be any known photo resist material, is deposited on the oxide layer 32. After using known masking and lithographic patterning techniques, a reactive ion etching, for example, is then performed on the photo resist layer 35 and the oxide layer 32. The reactive ion etching, in this step, may be selective to the oxide layer. This begins the process of forming the nFET channels 45. After the oxide etch, the Si layer 20 is selectively etched using a reactive ion etch. An optional amorphous Si etch may be performed to improve the etch quality. In one implementation, the channel 45 is etched to a depth of about 200Å to 400Å in the Si insulation layer 20. However, this depth may vary depending on the particular application used with the invention.

In an alternative step, the Si is first amorphized using a Ge implant at a typical dose of 2e14#/cm^2 to 1e15 #/cm^2 with an energy in the range of 10keV to 100keV depending on the depth of etches needed. This optional amorphization step may be used to improve the etch quality. In either fabrication, the channels 40 and 45 are formed in the Si layer 20 corresponding to a placement of the pFETs and nFETs, respectively. In one implementation, the channels 40 and 45 are etched to a depth of about 200Å to 400Å, in the Si layer 20. However, this depth may vary depending on the particular application used with the invention.

Figure 2c is representative of further fabrication processes in accordance with the invention. In these fabrication processes, a SiGe layer 45a is grown in the channels 45 of the nFET to a height of about 100 Å to 300 Å, although other heights are also contemplated by the invention. In one embodiment, the Ge content of the SiGe may be from 0% to 50% in ratio to the Si content, preferably about 15%. Then, an epitaxial Si layer 60 is selectively grown over the SiGe layer 45a in the nFET channels 45. A sacrificial gate oxide layer is then grown over the selectively grown Si layer 60. An nFET mask and well implant is then provided using any well known fabrication process. A gate oxide 65a is then formed in the nFET regions. A gate polysilicon 70a is then deposited followed by chemical mechanical polishing, well known to those of ordinary skill in the art, to produce the structure shown in Figure 2c.

This same process can then be used to form the pFET of the device, which may equally be represented by Figures 2b and 2c. Instead of SiGe the PFET structure incorporates Si:C. The final product is shown in Figure 2d which shows the PFET that

incorporates selective Si:C gate oxide 65b and gate poly 70b. The oxide 32 is stripped and standard CMOS processing may be used to continue the process. These include extensions, source and drain regions, silicide formation, nitride etch stop layers, contact processes, interconnects, etc.

In yet another embodiment of the invention, if the stress level of greater than approximately 3 GPa can be achieved in the channel from the SiGe material, then the SiGe material may be used in both the pFET and the nFET channels. This approach facilitates a large Ge content since it requires an unrelaxed system. Therefore, it is possible to use the SiGe deposition steps described for the pFET. It should be recognized, though, that the process (Ge%) window may be small because of competing needs such as high stress and dislocation issues. Since the stress levels with the channel are relatively reduced compared to the embedded material, the embedded material should have a larger Ge percentage than approximately 25% to 30%, in embodiments, to apply this structure for pFETs. In this approach, there is no independent pFET and nFET control.

Figure 3 illustrates the locations of the stresses in an nFET device according to the invention. As shown in Figure 3, tensile stresses are present in the channel of the nFET with a region of unrelaxed SiGe under compression. More specifically, in the structure of the invention, the lattice structure of the SiGe layer 45a matches the lattice structure of the underlying Si insulation layer 20. This results in the SiGe layer 45a and the surrounding areas being under a compressive stress. The surrounding areas will try to

obtain an equilibrium state thus resulting in a tensile stress of the epitaxial Si layer 60 formed on the SiGe layer 45a.

Figure 4 illustrates the locations of the stresses in a pFET device according to the invention. As shown in Figure 4, compressive stresses are present in the channel of the pFET with a region of unrelaxed Si:C under tension. More specifically, in the structure of the invention, the lattice structure of the Si:C layer 40a will match the lattice structure of the underlying Si insulation layer 20. This results in the Si:C layer 40a and the surrounding areas being under a tensile stress. As in the occurrence with the SiGe layer, the surrounding areas of the Si:C layer 40a will obtain an equilibrium state. This, however, results in a compressive stress of an epitaxial Si layer 60 formed on the Si:C layer 40a.

In one implementation, the preferred range of the longitudinal stress component (stress in direction of current flow from source to drain) in the Si epi 60 of the nFET, of Figure 1f, is a tensile value greater than 100MPa while in the pFET Si channel a compressive value greater than 100MPa is preferred.

Thus, in the structure of the invention, tensile stresses are now formed in the channel of the nFET and compressive stresses are formed in the pFET. In one implementation, high tensile stresses can also be formed in the pFET. By allowing such stresses, high device performance can be achieved. In addition, with the processes of the invention, the manufacturing costs can be reduced with resulting higher yields.

While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims. For example, the invention can be readily applicable to bulk substrates.